

Design and Implementation of Reversible Multiplier using optimum TG Full Adder

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Abstract: *The reversible logic has received great attention in last few years due to their ability to reduce the power dissipation which is the main requirement in low power VLSI design. Multipliers are widely used in DSP for calculation of FFT, convolution, to perform MAC operation, and in microprocessors to perform ALU related operations. This paper proposes a 16X16 reversible multiplier using Toffoli gate Full adder which can multiply two 16-bit numbers. It is based on the two concepts, the partial products are generated in parallel using Toffoli gates, and the addition of partial products is carried out by using reversible full adder designed with modified TG gate. The designed multiplier is faster and has low hardware complexity. In addition to that the designed reversible multiplier is better than the existing counterparts in terms of power consumption, delay, Garbage inputs, outputs, and quantum cost. The designed 16-bit multiplier is modeled using Verilog HDL and functionality is verified with Xilinx Vivado 2016.2.*

Keywords: *Reversible Logic, Reversible Gate, Power Dissipation, Garbage.*

I. Introduction

In irreversible logic computations, each bit of information lost generates $kT \ln 2$ joules of heat energy, where k is Boltzmann's constant and T the absolute temperature at which computation is performed [1-2]. Bennett showed that $kT \ln 2$ energy dissipation would not occur if the computation was carried out in a reversible manner [3], since the amount of energy dissipated in a system bears a direct relationship to the number of bits erased during computation. Reversible circuits are the circuits that do not lose information and reversible computation in a system can be performed only when the system consists of reversible gates. In reversible logic there is one-to-one mapping between the input and output vectors and vice-versa. Reversible logic has greater applications in the fields of high speed power aware circuits, low-power CMOS design, optical computing, nanotechnology and quantum computing [4]. Multipliers play an important role in today's digital signal processing and various other applications. With advances in technology, the major design constraints of a multiplier are high speed, low power consumption, regularity of layout and hence less area or even combination of them in one multiplier thus making them suitable for various high speed, low power and compact VLSI implementation. Generally, multipliers are used in Digital Signal Processor (DSP)'s for calculation of FFT, convolution, and to perform MAC operations, Microprocessors in ALU based operations etc. This paper proposes a 16x16 Braun array multiplier designed using reversible Toffoli Gate Full Adder. One of the major goals in reversible logic design is to minimize the number of reversible gates and garbage outputs (garbage outputs are the unutilized outputs required to maintain reversibility). There are plenty of gates available in reversible logic. But, in the proposed design Toffoli gate is used, Because of its low quantum cost and less number of garbage outputs [5]. A new reversible gate termed Modified Toffoli Gate (MTG) is used in the design of multiplier, because of less number of reversible gates and garbage outputs. Then compared the performance parameters of Braun multiplier with previously designed multipliers using HNG [6], PFAG [8], PG and TG [9] gates. This paper is organized as follows. Section II deals with the basic reversible gates, section III shows the proposed designs of 4x4, 8x8, 16x16 multipliers respectively. Section IV deals with results and discussion. Finally, conclusion is presented in section V.

II. Reversible Logic Gates

It has been proved that, "Losing information in a circuit causes losing power [1-3]. Information lost when the input vector cannot be uniquely recovered from the output vector of a combinational circuit". The gate/circuit that does not lose information is called reversible. A reversible logic gate is an N-input, N-output logic device that provides one to one mapping between the input and the output [5]. It not only helps us to determine the outputs from the inputs but also helps us to recover the inputs from the outputs. Quantum cost [8] refers to the cost of the circuit in terms of the cost of a primitive gate. Gate count [14] is the number of reversible gates used to realize the function. The unutilized outputs from a reversible gate are called "garbage outputs".

While constructing reversible circuits with the help of reversible logic gates, some restrictions should be strictly maintained:

- Loops are not permitted.
- Fan-out is not permitted

The following are the important design constraints for reversible logic circuits [7].

1. Reversible logic circuits should have minimum quantum cost.
2. The design can be optimized so as to produce minimum number of garbage outputs.
3. The reversible logic circuits must use minimum number of constant inputs.
4. The reversible logic circuits must use a minimum logic depth or gate levels.

Reversible logic has extensive applications in future emerging technologies such as quantum computing [4], optical computing as well as ultra low power VLSI circuits, DNA computing to produce zero power dissipation under ideal conditions. Reversible logic is very essential for the construction of low power, low loss computational structures which are very essential for the construction of arithmetic circuits used in quantum computation, nanotechnology and other low power digital circuits. Recently, several researchers have focused their efforts on the design and synthesis of efficient reversible logic circuits [15]. Reversible implementations are also found in thermodynamics and adiabatic CMOS [11]. Power dissipation in modern technologies is an important issue, to reduce the power dissipation using reversible logic [16].

a) Toffoli Gate [1]

A Reversible gate has equal number of inputs and outputs. A reversible circuit consists only reversible gates with no fan-out or feedback. Constant inputs in a reversible circuit are referred to as Ancilla inputs and Garbage outputs are those outputs which is neither primary nor useful outputs. The inputs regenerated at the outputs are not garbage outputs. Some of the reversible gates are PERES [9], TOFFOLI [11], CNOT/FEYNMAN [12] and FREDKIN [13] gate. Among them the most useful gate was TOFFOLI gate, because of its low quantum cost and less number of garbage outputs [11]. An $n \times n$ Toffoli gate is shown in figure 1, maps the input vector $[n_1, n_2, n_3 \dots n_k]$ to the output vector $[O_1, O_2, O_3 \dots O_k]$, where $O_j = n_j$ (for $j=1, 2 \dots k-1$) and the first $(n-1)$ bits are called control lines and last bit is called target line. Here the target bit is toggled only when all control lines are '1'. The Toffoli gate is having the quantum cost of 5 and with a delay of 5Δ .

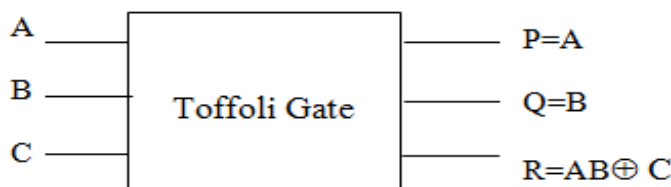


Fig.1: Toffoli Gate

Table 1: Truth Table of Toffoli gate

| Inputs | | | Outputs | | |
|--------|---|---|---------|---|---|
| A | B | C | P | Q | R |
| 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 | 0 | 1 |
| 0 | 1 | 0 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | 1 | 1 |
| 1 | 0 | 0 | 1 | 0 | 0 |
| 1 | 0 | 1 | 1 | 0 | 1 |
| 1 | 1 | 0 | 1 | 1 | 1 |
| 1 | 1 | 1 | 1 | 1 | 0 |

b) Full Adder Design Using TG gate

I. Design of single bit TG adder

The internal design of a single bit TG full adder is shown in figure 2. In this the TG gate is modified to get the full adder functionality, by adding an extra input i.e., constant input '0'. Number of garbage outputs obtained from the design are 2. Single TG gate is required for the design of single bit TG full adder. Quantum cost of the single bit TG adder is 12.

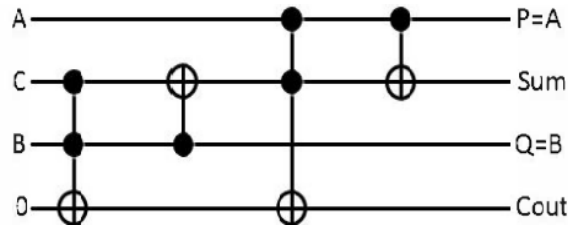


Fig. 2: Design of single bit TG adder

Table 2: Truth table of single bit TG adder

| Inputs | | | | Outputs | | | |
|--------|---|---|---|---------|---|-----|------------------|
| A | B | C | D | P | Q | SUM | C _{out} |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 |
| 0 | 1 | 0 | 0 | 0 | 1 | 1 | 0 |
| 0 | 1 | 1 | 0 | 0 | 1 | 0 | 1 |
| 1 | 0 | 0 | 0 | 1 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 | 1 | 0 | 0 | 1 |
| 1 | 1 | 0 | 0 | 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 |

II. Design of 4-bit TG Adder

The internal design of a 4-bit TG adder is shown in figure 3. There are four single bit TG adders are required to design a 4-bit TG adder. Number of constant inputs used in the design are 4. The number of Garbage outputs obtained from the design is 8 and the quantum cost of a 4-bit TG adder is 48.

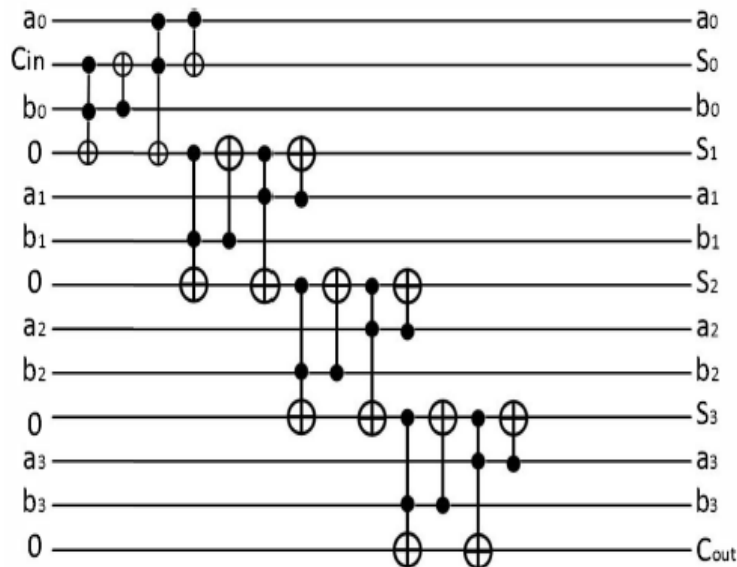


Fig. 3: Design of 4-bit TG adder

III. Design of Braun Multiplier

I. Braun Multiplier

The architecture of a 4*4 standard Braun multiplier is as shown in figure 5. In general, for an n*n Braun multiplier [10], there will be n (n-1) number of full adders and n² AND gates are required. This paper, proposes a reversible multiplier designed using reversible TG gate full adder. The multiplication of two 4x4 numbers are carried out in two steps. Step 1 involves the generation of the partial products. The summation of partial products is carried out using TG full adder in step 2.

a. Partial product generation circuit: Partial product generation of an n*n multiplier requires n*n AND operations. To compute the partial products for 4*4 reversible multiplier, this design needs 16 reversible gates to perform 16 AND operations. From figure 4 to perform each AND operation, a constant value of logical zero is applied as input to C. That will be the third input of TG gate to perform AND from the reversible TG

gate. Totally 16 partial products are generated to perform the multiplication of two 4-bit numbers. The use of Toffoli gate is to reduce the overall quantum cost of the circuit as well as the gate count.

b. Summation of partial products: After generating the partial products, to perform the summation operation 12 full adders (FA) are required. The Full adder is designed using a reversible gate i.e., Toffoli gate. Basically, Toffoli gate is a 3*3 gate, but to get the full adder output this will be changed to a 4*4 gate by adding a constant input of '0' given as extra input. Generally, the carry input of full adder is dependent on the carry output of the previous full adder. Hence, the delay is more for the ripple carry adder. The delay and power dissipation of the multiplier can be reduced by replacing the Non reversible logic gates with reversible logic gates like Toffoli gates.

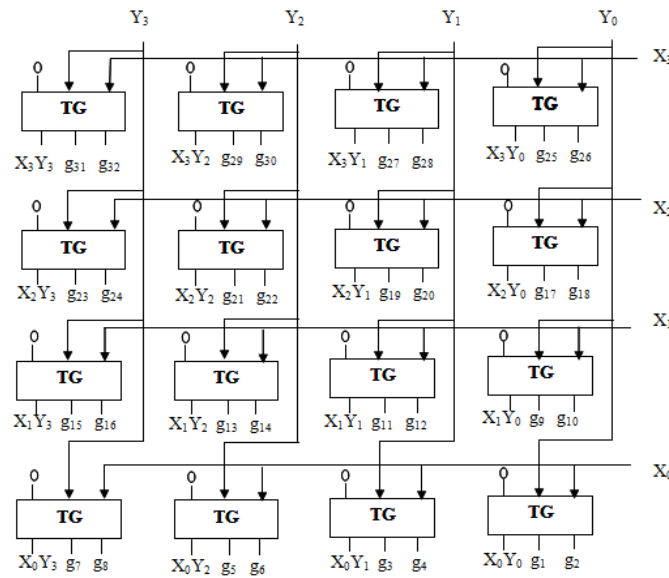


Fig. 4: Partial Products generation by using Toffoli gate

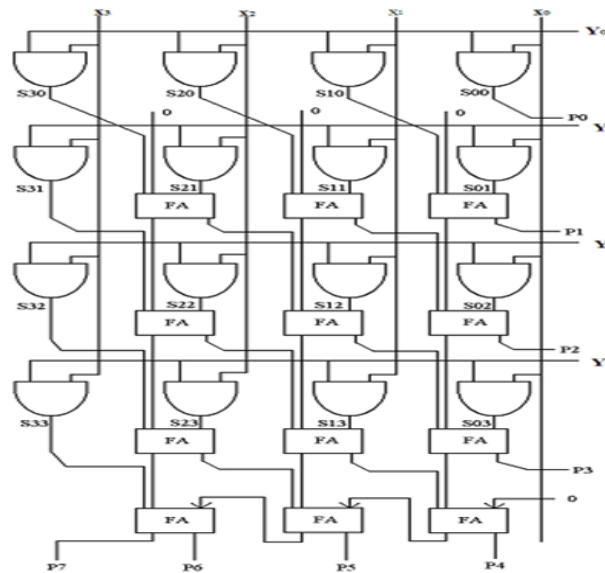


Fig. 5: 4x4 Braun multiplier

II. Block Diagram of 8x8 Braun multiplier

The block diagram of 8x8 Braun multiplier is shown in figure 6. Four 4x4 multipliers and three 8-bit adders are used in the design of an 8x8 Braun Multiplier. The first multiplier will multiply the terms a[3:0] and b[3:0]. The product value of first multiplier lower 4 bits will generate the final product bits P₀-P₃, and the remaining 4-bits will be given as inputs to the second 8-bit adder. Then the second multiplier multiply the terms a[7:4] and b[3:0], and the third multiplier multiply the terms a [3:0] and b[7:4]. The product values of these two

will be given as inputs to a first 8-bit adder. The output of this adder will be given as input to the second 8-bit adder. The fourth multiplier will multiply the terms $a[7:4]$ and $b[7:4]$. The product value of this multiplier will be given as input to the third 8-bit adder. The output of the second 8-bit adder lower 4-bits will generate the final product bits P_4-P_7 , and the third 8-bit adder will generate the product value of $P [15:4]$. The final product will contain 16-bits.

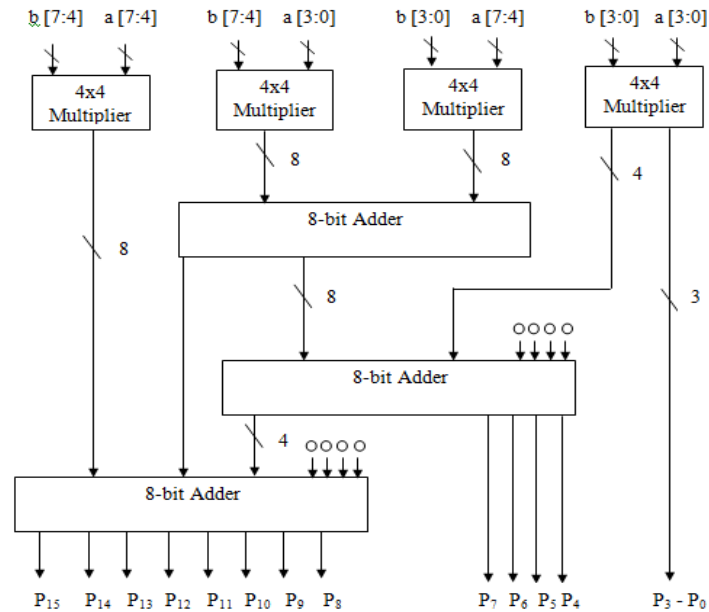


Fig. 6: Block Diagram of 8x8 Braun Multiplier

III. Block Diagram of 16x16 Braun multiplier

The block diagram of 16x16 Braun multiplier is shown in figure 7. Four 8x8 multipliers and three 16-bit adders are used in the design of a 16x16 Braun Multiplier. The first multiplier will multiply the terms $a [7:0]$ and $b [7:0]$. The product value of first multiplier lower byte will generate the final product bits P_0-P_7 , and the remaining higher byte will be given as input to the second 16-bit adder. Then the second multiplier multiply the terms $a [15:8]$ and $b [7:0]$, and the third multiplier multiply the terms $a [7:0]$ and $b [15:8]$. The product values of these two will be given as inputs to a first 16-bit adder. The output of this adder will be given as input to the second 16-bit adder. The fourth multiplier will multiply the terms $a [15:8]$ and $b [15:8]$. The product value of this multiplier will be given as input to the third 16-bit adder. The output of the second 16-bit adder lower byte will generate the final product bits P_8-P_{15} , and the third 16-bit adder will generate the product value of $P [16:31]$. The final product will contain 32-bits.

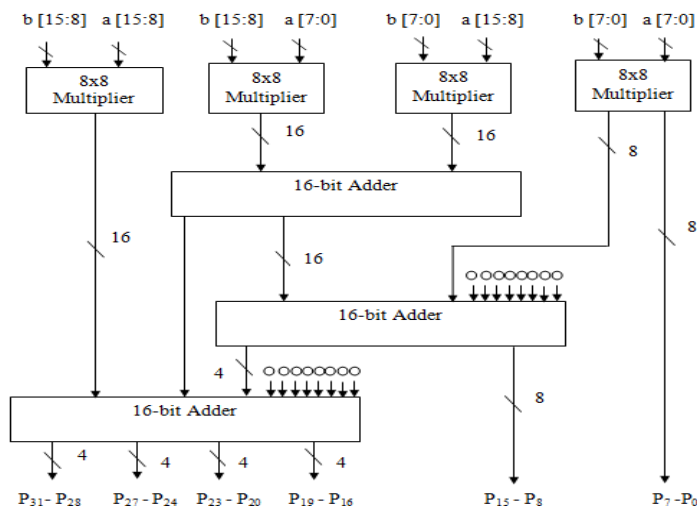


Fig. 7: Block Diagram of 16x16 Braun multiplier

IV. Results and discussion

The designed multipliers are modeled using Verilog HDL. The functionality is verified using Xilinx Vivado 2016.2 design suite. The simulated waveforms of 4x4, 8x8 and 16x16 reversible Braun multiplier are shown in figures 8, 10, 12 respectively. The design is implemented on Artix-7 FPGA. Synthesis is performed using Vivado Synthesis tool.

i. Simulation wave forms of 4x4 Braun Multiplier

Simulated waveforms of a 4x4 Braun Multiplier is shown in figure 8. a[3:0], b[3:0] are the two input variables and P[7:0] is an output variable.

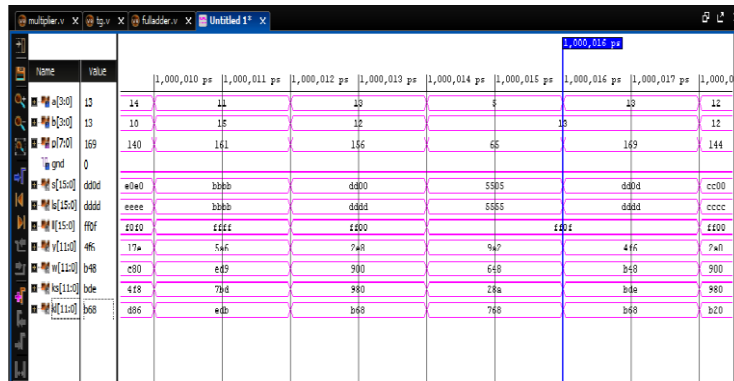


Fig. 8: Simulation wave forms of 4x4 Braun Multiplier

ii. RTL view for 4x4 Braun multiplier

The RTL view of 4x4 Braun Multiplier is shown in Figure 9. 12 single bit adders and 16 AND gates are required in the design of a 4x4 Braun multiplier.

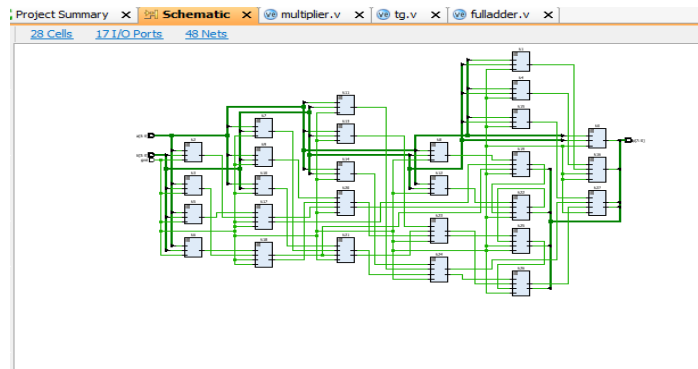


Fig. 9: RTL View for 4X4 Braun multiplier

iii. Simulation wave forms of 8x8 Braun Multiplier

Simulated waveforms of a 8x8 Braun multiplier is shown in figure 10. a[7:0], b[7:0] are the two input variables and P[15:0] is an output variable.

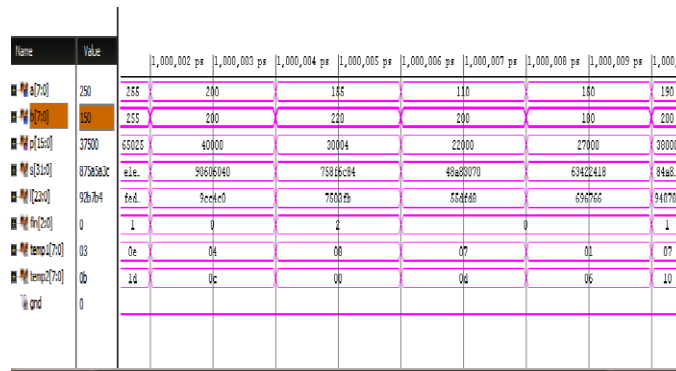


Fig. 10: Simulation Waveform for 8x8 Braun multiplier

IV. RTL view for 8x8 Braun multiplier

The RTL view of 8x8 Braun Multiplier is shown in Fig. 11. 12 single bit adders and 16 AND gates are required to design a 4x4 Braun multiplier. There are four 4x4 multipliers are used to perform an 8x8 multiplication.

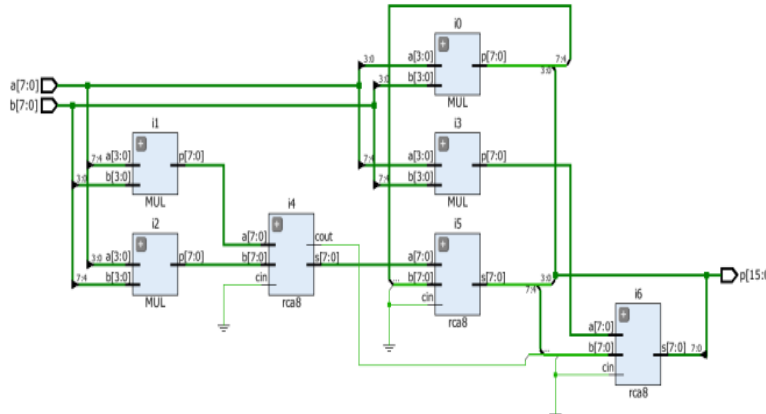


Fig. 11: 8x8 Braun Multiplier RTL view

v. Simulation wave forms of 16x16 Braun Multiplier

Simulated waveforms of a 16x16 Braun Multiplier is shown in figure 12. a[15:0], b[15:0] are the two input variables and P[32:0] is an output variable.



Fig. 12: 16x16 Braun Multiplier Simulation waveforms

VI. RTL view for 16x16 Braun multiplier

The RTL view of 16x16 Braun Multiplier is shown in Figure 13.

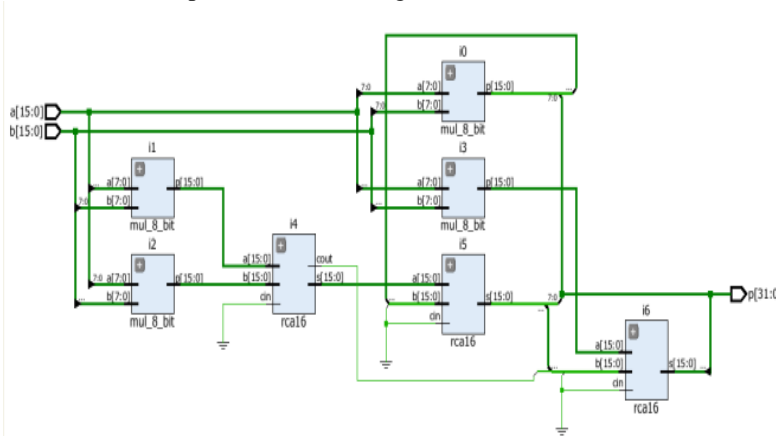


Fig.13: 16x16 Braun Multiplier RTL view

Table 3 gives the I/O utilization of designed multiplier.

Table 3: Comparison of cell, nets, I/O port usage for 4x4, 8x8, 16x16 multipliers

| Bit size of Braun Multiplier | Cell usage | nets | I/O ports |
|------------------------------|------------|------|-----------|
| 4x4 | 28 | 48 | 17 |
| 8x8 | 60 | 104 | 42 |
| 16x16 | 134 | 226 | 98 |

The comparison of the performance parameters are given in table 4, and table 5 gives the power consumption and delay of designed multiplier.

Table 4: Comparison of performance parameters with previous results

| Name of parameter | Braun Multiplier using Toffoli Gate (This work) | | | Array Multiplier using HNG [6] gate (4x4) | Array Multiplier using PFAG [8] gate (4x4) | Array Multiplier using PG & TG [9] gates (4x4) |
|----------------------|---|-----|-------|---|--|--|
| | 4x4 | 8x8 | 16x16 | | | |
| Garbage Inputs | 12 | 27 | 57 | 44 | 28 | 28 |
| Garbage outputs | 32 | 70 | 146 | 52 | 52 | 28 |
| Quantum cost | 144 | 296 | 614 | 160 | 152 | 153 |
| No.of Gates required | 28 | 59 | 121 | 44 | 28 | 36 |

Table 5: Power consumption and delay of 4x4, 8x8 and 16x16 Braun multipliers

| Bit size | Power (mW) | Delay (nS) |
|----------|------------|------------|
| 4x4 | 13.70 | 15.52 |
| 8x8 | 16.77 | 21.99 |
| 16x16 | 34.53 | 42.91 |

VI. Conclusion

The performance parameters like Garbage inputs, Quantum cost, Garbage outputs and number of gates are analyzed. Garbage outputs in the designed Braun multiplier are reduced when compared to HNG [6], PFAG [8] gate multipliers are 38%. Quantum cost in the designed Multiplier is also reduced when compared to HNG [6], PFAG [8], PG and TG [9] gates are 10%, 5.2%, 5.8% respectively. Number of gates in the designed multiplier is also reduced when compared with the multipliers of HNG [6], PG& TG [9] gates are 57%, 22% respectively.

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